

EXPERIENCE

2015–today muse.ai Worldwide

Co-Founder and CTO

- Pivoted the company's focus into applying the latest Artificial Intelligence technologies to enable Video Search
- Designed and implemented a proof-of-concept Video Search service, as well as a myriad of other systems
- Refined Machine Learning methodologies to improve the understanding of auditory and visual content
- Created guidelines and processes to hire, train, and increase the productivity of the team

2011–2015 Morgan Stanley London

EAI - Accelerator Group

- Member of the strategic group responsible for cross-technology libraries and platforms used by the entire firm
- Created a state-of-the-art platform for Rapid Hardware Development bridging a number of software development concepts with hardware design methodologies
- Designed and implemented a proof-of-concept for an Ultra-Low-Latency FPGA-based trading system including IP Cores for: UDP/IP, Book Building with Ultra-Fast Order Sorting, Matching and Crossing Engine with Pricing and Crossing rules
- Proposed and guided an academic collaboration which resulted in the creation of ScalaHDL and an IEEE paper
- Implemented a documentation scheme that extracts text and examples directly from source code
- Designed and implemented a Graph Database using MongoDB with a reactive web-based front-end for suggestive and intuitive graph traversal
- Managed teams to successfully deliver a myriad of projects including: a Total Order Communications Scheme; ULL FPGA-based Memory Cache-system; PubSub bridge used for market data distribution; benchmark a range of SerDes schemes (e.g. SBE, GPB, Fast, C-structs)
- Actively engaged in recruiting and mentoring new hires including talks at Imperial College and Oxford University

2010–2011 J. P. Morgan and Chase Co. London

Analytics Strategic Group

- Member of the Athena Core team which is responsible for developing, maintaining, and supporting a state-of-the-art platform for trading and risk reporting. This system included the trade-model; a globally replicated high performance database (C++), a graph-based RAD programming language (on top of Python) with a custom IDE, and the entire surrounding ecosystem with its scheduler, logging, GUI-widgets, web services, and messaging

2010–2010 Imperial College London London

Research Assistant

- Collaborated with the Embedded Optimization for Resource Constrained Platforms (EMBOCON) initiative to accelerate the heavy computational requirements for finding the optimal control moves
- Collaborated with the Novo-G Supercomputer initiative to build the most powerful reconfigurable computer

2008–today WebCanvas dot-com Ltd. London

Founder and CEO

- Invented and developed the [WebCanvas](http://webcanvas.com) - *The World's Largest Collaborative Painting* – <http://webcanvas.com>
- Project featured around the globe in a wide range of publications and T.V. shows including the BBC's Click Show

GNSS - Embedded Systems Engineer

- Presented work at NASA's Office of Digital Design conference MAPLD 2005 Int. Conference: [submission 168](#)
- Developed hardware (FPGA design) and software (Low-Level drivers) that are space-borne onboard [GIOVE/A](#)
- Developed a C++ GUI application to process and visualize data originating from a space qualified GPS receiver
- Assembled and tested band-pass filters for GPS signals

Junior Satellite Engineer

- Pioneer in the [Student Space Exploration & Technology Initiative](#)
- Participated in [European Space Agency's 4th Student Parabolic Flight Campaign](#)
- Coded in C and OpenGL a 3D simulation of the effects of electrical fields on a charged particle in Zero-Gravity

PUBLICATIONS & TALKS**Ph.D. Thesis**

- Accelerating Iterative Methods for Solving Systems of Linear Equations using FPGAs, Imperial College, 2010
The application of these methods was demonstrated using state-of-the-art Model Predictive Control systems

Papers

- ScalaHDL: Express and Test Hardware Designs in a Scala DSL, ICCD 2014: 521-524, 2010
- A High Throughput FPGA-Based Floating Point CG Implementation for Dense Matrices, TRET3 3(1) (2010)
- A Fused Hybrid Floating-Point and Fixed-Point Dot-Product for FPGAs, ARC 2010
- More Flops or More Precision? Accuracy Parameterizable LE Solvers for Model Predictive Control, FCCM 2009
- A High Throughput FPGA-based Floating Point Conjugate Gradient Implementation, ARC 2008
- A Floating-point Solver for Band Structured Linear Equations, FPT 2008
- FPGA Design of an Integrated CAN and EDAC for Spacecraft Applications – NASA, MAPLD 2005

Talks

- How Artificial Intelligence Sees, Hears, and Relates Concepts – Lisbon, 16/11/2017
- Modern Big Data Systems for Machine Learning – London, 10/07/2015
- Scala in Finance – Open Source Quantitative Finance – London, 02/04/2015
- The Bitcoin Innovation – University of Oxford – Oxford, 28/10/2014
- FPGAs in Finance – Imperial College London – London, 14/10/2014
- STAC - Hardware Acceleration Today – London, 04/12/2013
- Next Generation Networks – The Path to Zero Latency – London, 17/09/2014
- Bitcoin Analytics and Statistics – Python for Quants – New York, 14/03/2014
- What is Web 2.0 and how it changes almost everything – London, 14/05/2009
- More FLOPS or More Precision? Equation Solvers for Model Predictive Control – London, 23/03/2009
- An FPGA-Based Floating Point Solver for Band Structured Linear Equations – London, 23/03/2009
- Conjugate Gradient: Optimizing FPGA Speed using Custom Precision – London, 19/11/2008

EDUCATION

2014-2015

CQF Institute

London

Certificate In Quantitative Finance

- Highly comprehensive and pragmatic quantitative course divided into 6 modules with a final project
- Final project involved the implementation of a portfolio analysis and construction using Black-Litterman

2006-2010

Imperial College London

London

Ph.D. in Accelerating the Iterative Methods using FPGAs

- Research was focused on accelerating the solution of systems of linear equations in the context of Quadratic Programming for Model Predictive Control. Presented research in [London](#), [Taipei](#), [Bangkok](#), [Napa](#), [Belfast](#), ...
- Results achieved at least an order of magnitude improvement when compared to high-spec computer systems

2002-2006

University of Surrey

Guildford, UK

Electronics and Computer Engineering

- Graduated top of the class with First Class Honours
- Presented at NASA's Digital Design Conference in [Washington D.C.](#)

OTHER INTERSTS & HOBBIES



ERDÖS NUMBER: 4



Antonio Roldao Lopes



George A. Constantinides



Gerhard J. Woeginger



Ulrich Faigle



Paul Erdos